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# Switching Transient Analysis and Characterization of GaN HEMT

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**Abstract**—High electron mobility transistor (HEMT) has the advantage of fast switching capability, low power loss and small package design. Gallium Nitride (GaN) HEMT is widely researched in recent years. Accurate characterization and detailed switching analysis are critical for the practical application in power converters. In this paper, a 650V GaN HEMT is tested based on the double pulse tester. Based on the experimental results, the switching transient analysis is given and the phenomenon of Miller plateau shifting is explained. Switching time and switching loss characterization are given as the reference value for converter design.

**Keywords**—double pulse test; GaN HEMT; Miller plateau; switching characterization

## I. INTRODUCTION

As the development of Silicon semiconductors has reached its physical boundary, wide band-gap devices are considered as the next generation of semiconductor transistor [1]. GaN HEMT shows a promising potential in the fabrication of high frequency and high power density converter, which has been widely researched during the last decade [2], [3]. The basic structure of GaN HEMT can be plotted as the equivalent circuit shown in Fig. 1 [4].

Gating characterization and switching loss characterization are two major concern for the transistor application [5]. Gating characterization is decided by the transistor input capacitor ( $C_{iss}=C_{GS}+C_{GD}$ ). Switching loss characterization is decided by the transistor output capacitor ( $C_{oss}=C_{DS}+C_{GD}$ ) [6]. Benefit from wide semiconductor band-gap, GaN HEMT has a lower parasitic capacitor and lower conduction resistance than their Silicon counterparts, which leads to fast switching capability and low switching loss [7]-[9]. Accurate characterization of transistor switching loss and switching time is important for converter efficiency and modulation design. As a result, switching transient analysis of GaN HEMT is essential.

Double pulse test is a practical method for characterizing the transient performance of semiconductor transistor [10], [11]. Accuracy of the test result is highly dependent on the gate loop and power loop layout in the printed circuit board (PCB), as well as measurement technique [12]. Double pulse test has been carried out to characterize the switching loss of GaN HEMT [13], [14]. However, switching time characterization is not given. In addition, detailed analysis of the switching transient is absent.

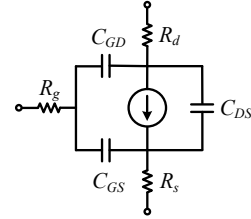


Fig. 1. Equivalent circuit of GaN transistor.

In this paper, double pulse test of 650V GaN HEMT is carried out. Switching transient is analyzed and Miller plateau shifting phenomenon is explained. Switching loss and switching time characterization are given, which can be used as the reference value for converter design. The paper is arranged as follows: Section II introduces the double pulse tester design. Switching characterization and Miller plateau shifting phenomenon are explained in Section III. Section IV concludes the paper.

## II. DOUBLE PULSE TESTER

Equivalent circuit of double pulse tester is plotted in Fig. 2. GS66516B (e-mode, 650V) from *GaN System* is selected as the device under test. Among all these parasitic parameters, minimization of source inductance ( $L_s$ ) and gate inductance ( $L_g$ ) are the primary concern, which directly determines the transistor switching performance.

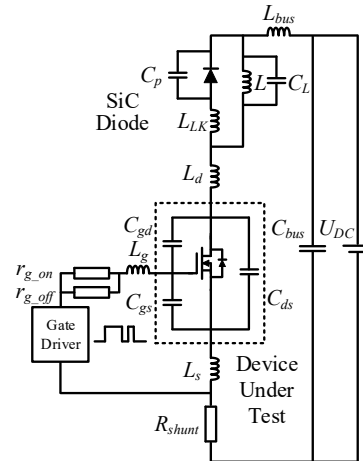


Fig. 2. Equivalent circuit of the double pulse tester.

For GS66516B, Kelvin connection is adopted for the source pad design, which minimizes the  $L_s$ . For gate loop PCB design, special attention has been paid for the low impedance design, which minimizes the  $L_g$ . Operating principle of the double pulse test is shown as follows. Inductor  $L$  is charged by the DC source when the transistor is gated on. The first pulse excites  $L$  to a desired operating current and SiC Diode maintains the current flowing between the two pulses. The turn-on transient of the second pulse shares the same switching condition with the turn-off transient of the first pulse, which are thus used for switching characterization. Design method and measurement technique of the test are detailed as follows.

#### A. Gate Loop Design

Gate loop is the charging/discharging path of the transistor input capacitor, which directly determines the gate driving wave pattern. Gate resistors are generally installed to limit the gate charge/discharge current, which can be noted as (1), where  $U_g$  is the on-state gate voltage and  $U_{PL}$  is the voltage of Miller plateau. With a small gate resistance, large gate current can shorten the transistor switching transient, while, on the other hand, leads to extra ringing in the driving signal.

$$I_{charge} = \frac{U_g - U_{PL}}{r_{g\_on}}, I_{discharge} = \frac{U_{PL}}{r_{g\_off}} \quad (1)$$

The tolerance value of gate voltage is specified as -10V to +7V in the datasheet of GS66516B. Accordingly, a large gate-on resistor is adopted for switching safety and a small gate-off resistor is adopted for fast switching off. Experimental results of the gate driver signal with different gate-off resistors are shown in Fig. 3. A large ringing in the gate-off signal can be observed when gate-off resistor is removed. The ringing spike may lead to false turn on during the switching off transient, which must be avoided in the application of power conversion. Gate resistor is selected as a tradeoff between switching time and gate signal ringing. When  $r_{g\_on}=10\Omega$  and  $r_{g\_off}=2\Omega$ , the gate signal, shown in Fig. 3, is ideal for switching application, which is adopted in the gate loop design.

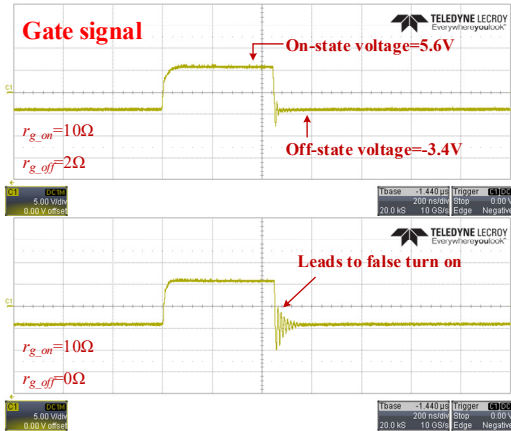


Fig. 3. Gate signal with different gate-off resistor.

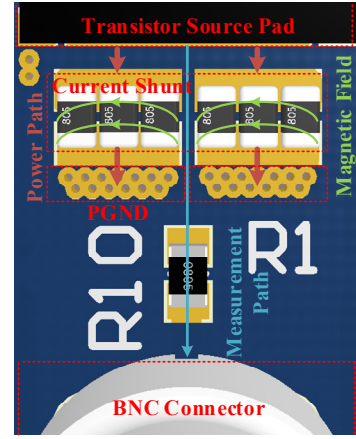


Fig. 4. PCB model of the current measurement method.

#### B. Measurement Technique

For transient analysis, wave pattern of  $U_{ds}$ ,  $I_d$  and  $U_g$  during the switching process must be accurately measured. Since the bulky clamp can introduce large parasitic inductance into the transistor power loop, conventional current probe cannot be applied. A minimized stray inductance current shunt method is adopted in this paper, which is shown as the 3D PCB model in Fig. 4. Paralleled resistors are installed to the source pad of the transistor. The symmetrical arrangement results in the magnetic field cancellation and thus creates a current measurement path free from electric magnetic interference, which improves the measurement accuracy [15]. A low parasitic capacitance voltage probe (7.5pF) is adopted for voltage measurement and ground clip is utilized to minimize the ground inductance loop. Detailed test specification is elaborated in the next section.

#### C. Double Pulse Tester

The fabricated double pulse tester is shown in Fig. 5. Air core inductor is used for current forming. A C2000 launchpad board is used to generate the double pulse gate signal. At 400V drain-source voltage, the transistor is driven from 5A to 30A. Drain current is sampled according to the shunt voltage drop and picked up through 50  $\Omega$  coaxial cable. Transient wave pattern and switching characterization are obtained.

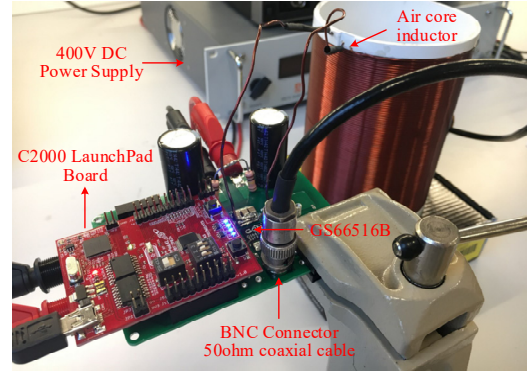


Fig. 5. Experiment set-up of double pulse tester.

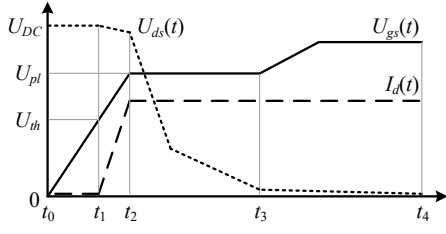


Fig. 6. Typical waveforms during transistor switch-on transient.

### III. SWITCHING CHARACTERIZATION

Switching transient analysis is of vital importance for the performance evaluation of transistor. Typical waveforms during transistor switch-on transient is shown in Fig. 6. Gate current first charges the  $C_{GS}$ . As gate voltage reaches the threshold voltage ( $U_{th}$ ), the transistor starts to partially gate on. During this period ( $t_1 \sim t_2$ ), transistor current rises up to the load current until  $C_{GS}$  is fully charged. After that, gate current starts to charge the  $C_{GD}$ , which is the well-known Miller plateau ( $t_2 \sim t_3$ ). When  $C_{GD}$  is fully charged, the gate voltage continues to rise until the on-state value ( $t_3 \sim t_4$ ). After that, the transistor is fully gated on and switching transient is ended. The overlapping area of  $U_{ds}(t)$  and  $I_d(t)$  during  $t_1 \sim t_3$  can be calculated as the switch-on loss. The switch-off transient is symmetrical the reverse process. Experimental results based on the double pulse tester are given as follows.

#### A. Switching Transient Analysis

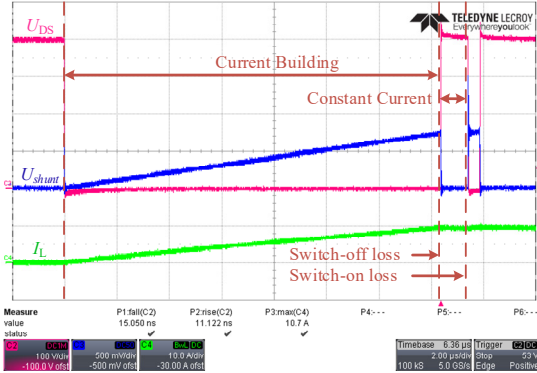


Fig. 7. Experimental waveforms of the double pulse test.

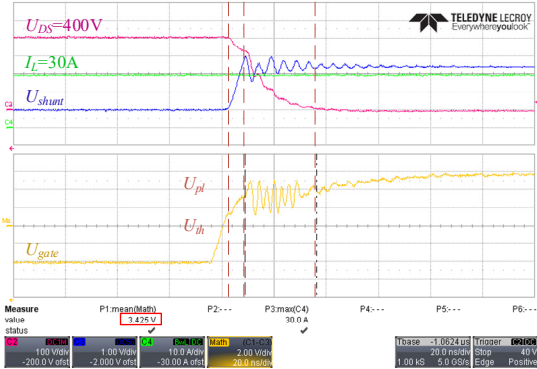


Fig. 8. Switch on transient at 400V, 30A.

Experimental waveforms during the complete double pulse test is shown in Fig. 7. The first pulse gates on the transistor and charges the inductor to 10A. Inductor current is circulating in the paralleled diode path and keeps constant during the interval between two gate pulses. The second pulse gates on the transistor again with the same switching condition. Switch-on and switch-off performance are characterized at the marked transient point.

Experimental waveforms of the switch-on transient at 400V, 30A is shown in Fig. 8. The waveforms are consistent with the theoretical analysis as well as the trend shown in Fig. 6. Switching transient is smooth, which validates the practical feasibility of the PCB layout design. Miller plateau voltage ( $U_{pl}$ ) is justified as 3.425V at this switching condition, which is calculated according to the average value during the whole plateau interval. Threshold voltage is justified as 1.3V, which is consistent with the value specified in the transistor datasheet.

#### B. Miller Plateau Shifting

Double pulse test is carried out in a wide current range (from 5A to 30A). According to the experimental results, an obvious shifting of Miller plateau can be observed in the higher current rate. To validate the observation, value of Miller plateau voltage is recorded during the all the tests, which is shown in Table I. It can be concluded that the Miller plateau voltage is higher when GaN HEMT switches at a higher current rate. According to (1), a higher  $U_{pl}$  will result in a lower gate-on current and higher gate-off current. As a result, characterization of the GaN HEMT gate-on and gate-off capability shall be different along different current rate. The switching time characterization of GS66516B is shown in Fig. 9. In a higher switching current, switch-on time is longer and switch-off time is shorter, which further validates the Miller plateau shifting phenomenon. It should be noted that the switch-off time at a lower current rate is much longer, which may interfere with the modulation scheme and leads to shoot-through in half bridge. Modulation dead time must be well designed in the application of power inversion, where current constantly crosses zero.

TABLE I. MILLER PLATEAU VOLTAGE CHARACTERIZATION

Current Rate (A)	5	10	15	20	25	30
Plateau Voltage (V)	2.90	3.05	3.22	3.29	3.35	3.43

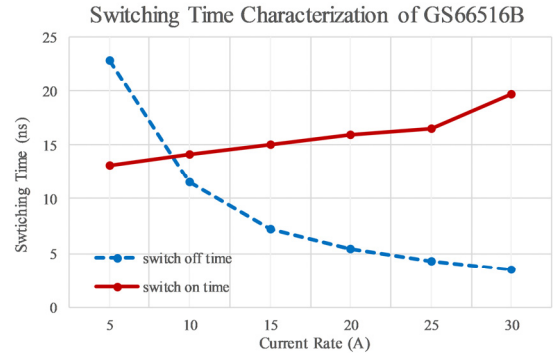


Fig. 9. Switching time characterization.

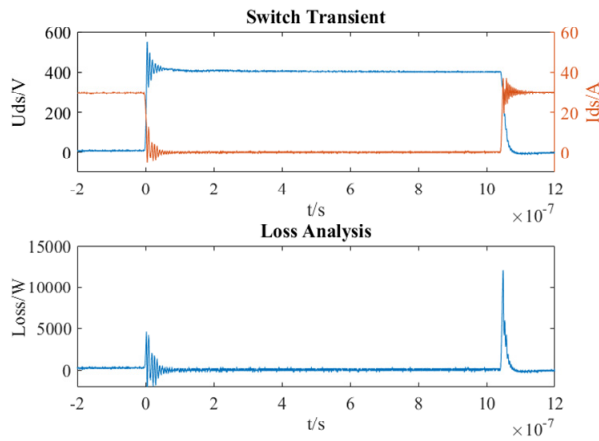


Fig. 10. Switching loss processed by MATLAB.

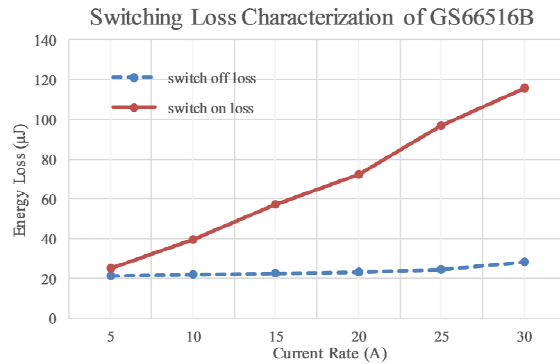


Fig. 11. Switching loss characterization.

### C. Switching Loss Characterization

Switching loss is the main cause of converter power dissipation, especially in high frequency application. Accurate characterization of transistor is important for converter efficiency and heat sink design. Double pulse test results are processed with MATLAB to obtain the switching loss, which is shown in Fig. 10.  $U_{ds}$  and  $I_d$  are sampled in 10Gb/s, and multiplied for instant power calculation. The instant loss power is integrated for 100ns in the vicinity of each switching transient to obtain the switching loss. Switching loss characterization of GS66516B is shown in Fig. 11. Switch on and switch off loss both increase with a higher current rate. Switch on loss is the major part of loss dissipation, which indicates the necessity of soft-switching technique in the high frequency application.

## IV. CONCLUSION

In this paper, a double pulse tester is fabricated for GaN HEMT devices. Gate loop design and current measurement technique are elaborated. GS66516B, as a template, is tested and switching transient analysis is given. The phenomenon of Miller plateau shifting is introduced and validated by the

switching time characterization. The switching loss characterization is given for converter design reference.

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